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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/800,764	03/06/2001	Aki Korhonen	PCDR-01004US0	3899

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/800,764	KORHONEN, AKI	
	Examiner	Art Unit	
	James C Kerveros	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,15-22 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,15-22 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a Non-Final Action in response to the Amendment and Remarks filed 11/19/2004, in reply to the Office Action mailed on March 1, 2004.

Claims 1-23 were rejected in the prior Office Action.

Claims 12-14 and 23 have been cancelled. Claim 24 was added.

Claims 1-11, 15-22 and 24 are now pending and presently under examination.

Response to Amendment

The petition under 37 CFR 137(b), filed November 19, 2004, to revive the present Abandoned Application, is GRANTED.

Objection to the drawings, with respect to data paths 105 and 107, has been withdrawn in view of the mark up corrections.

Objection to the drawings for figures 1 and 2, for lacking "Prior Art" legend, has been withdrawn in view of adding the "Prior Art" legend in Figure 1, while Figure 2 does not require prior art designation according to Applicant's remarks.

Rejection to the Claims under 35 U.S.C. 112, first and second paragraphs, is hereby withdrawn in response to canceling claims 12 and 23, in view of the Amendment to the claims.

Rejection to Claims 1-14, 22 and 23 under 35 U.S.C. 101 because of lacking utility, is hereby withdrawn in response to Applicant's arguments and claims amendment.

Response to Arguments

Applicant's arguments, see Amendment filed 11/19/2004, with respect to the rejections of claims as being anticipated by Cepulis et al. (US 6,463,550), and claims as being unpatentable over Cepulis et al. (US 6,463,550), have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

However, upon further consideration, a new ground of rejection is made in view of Kinzelman (U.S. Patent No. 6,144,930), as set forth in the present Office Action. Therefore, applicant's arguments with respect to claims 1-11, 15-22 and 24 are moot in view of the new ground of rejection.

Drawings

The drawings are still objected to, because the application lacks formal drawings due to hand written legends. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent,

except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4, 6-11, 15, 17-20, 22 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Kinzelman (U.S. Patent No. 6,144,930), issued: November 7, 2000, filed: June 9, 1993.

Regarding independent Claims 1, 15, 20, 22, 24, Kinzelman discloses a method and apparatus for detecting a defect in a computing system (Figure 1) including a central processing unit (CPU 12) and a system memory 14 logically partitioned into sections, comprising:

Loading a test program code in memory section 14e of the system memory 14 for testing the system memory, the test program code having a plurality of instructions configured to detect defects in the system memory, by using a section 14c to store the actual data obtained during the execution of the test program, whereas a section 14d is used to store the predicted data expected, and then comparing the actual data with the predicted data expected to determine whether any errors occurred during the execution of the test program.

Fetching and executing a fetched instruction of the test program code with the CPU 12, which executes the test program using the memory 14 available in the system. The CPU places the instructions from the test program on the bus, which accesses the appropriate sections of memory.

Determining whether the executed instruction yields a test result in conformance with an expected result, by performing a comparison between the contents of memory section 14c, containing the actual data, and the contents of memory section 14d, containing the predicted data, (step 43), Figure 4. If these contents are found to be equal at step 44, the process is repeated. If however, the values are unequal, an error message is printed at step 45 to a log file (not shown) to be used during debug of the system design and the test program stops executing. The message contains information regarding the error, which includes the address at which the error occurred, and the predicted (good) data, which should be contained at the address as well as the actual (bad) data that was found at the address.

Regarding Claim 2, Kinzelman discloses error message (step 45) contains information regarding the error, which includes the address at which the error occurred, and the predicted (good) data, which should be contained at the address as well as the actual (bad) data that was found at the address.

Regarding Claim 4, Kinzelman discloses execution of a simulation, Figure 4, where the predicted effect of the transaction on the memory model is determined by the test program at step 42a and the predicted data is stored in the memory 14 at a location in memory section 14d.

Regarding Claim 6, Kinzelman discloses Figure 3, step 34, a pointer 15c.sub.i ' to the location of the memory assigned to the memory model is stored within the memory model itself. The results, if any, from the transaction are provided to the test program and the test program stores the results in a location of memory section 14c

corresponding to an address contained in the respective pointer 15c.sub.i ' in the particular memory model 15c.sub.i.

Regarding Claims 7, 8, 9, Kinzelman discloses the predicted effect of the transaction on the memory model is determined by the test program at step 42a and the predicted data is stored in the memory 14 at a location in memory section 14d. The predicted as well as actual data resulting from such transactions are stored in the memory sections 14c and 14d.

Regarding Claims, 10, 11, with respect to claimed limitation of the execution run time, Kinzelman describes in the Background of the Invention, that execution of the software models and test programs can dominate use of a simulation computer system's resources and moreover, take a very long time to complete execution. Usually, test programs are very CPU intensive, that is the test programs use large blocks of time in the CPU.

Regarding Claims 17-19, Kinzelman discloses a computer system as it is well known in the art, which generally comprised a central processing unit (CPU), a memory unit, at least one input/output (I/O) device, and a bus for connect the aforementioned devices. Typical types of I/O devices include among others, "displays" for reporting to a computer user, message containing information regarding the error, which includes the address at which the error occurred, the predicted (good) data which should be contained at the address as well as the actual (bad) data that was found at the address, see Background of the Invention, and Figure 4, step 45.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 5, 16 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzelman (U.S. Patent No. 6,144,930) inn view of Barr (U.S. Patent No. 5,758,056).

Regarding Claim 3, 16, 21, Kinzelman does not explicitly disclose, "de-allocating a portion of the system memory upon determining that the portion is defective and removing a CPU upon determining that the CPU is defective". However, in analogous art, Barr (U.S. Patent No. 5,758,056) discloses a memory system having defective address identification and replacement, including a replacement memory 18 for replacing defective bits within the main memory 17. Thus full functionality is restored to the main memory by substituting functional bits within the replacement memory for defective bits within the main memory.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to replace defective bits within the system memory of Kinzelman using a replacement memory as taught by Barr, for the purpose of restoring full functionality to the main memory by substituting functional bits within the

replacement memory for defective bits within the main memory. A person skilled in the art would have been motivated to do so, since repairing a defective memory location is accomplished without removing the memory module from the host computer system. Furthermore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to remove a defective CPU and replace it with a good one, since it is well known in the art, that a defective CPU would not be able to execute the required instructions for storing information in the main memory.

Regarding Claim 5, Kinzelman does not explicitly disclose switching a CPU. In an analogous art, Barr (U.S. Patent No. 5,758,056) discloses a memory system having defective address identification and replacement, including a replacement memory 18 for replacing defective bits within the main memory 17. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to remove a defective CPU and replace it with a good one, since it is well known in the art, that a defective CPU would not be able to execute the required instructions for storing information in the main memory.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

By: 3/16/06

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Office Action: Non-Final Rejection